microelectronic element and one or more edge surfaces extending between said top and bottom surfaces, and then

selectively forming elongated flexible bond ribbons over said compliant layer so that said bond ribbons extend over said top surface and one or more of said edge surfaces and said bond ribbons electrically connect said contacts to conductive terminals overlying the top surface of said compliant layer.

22. The method as claimed in claim 21, wherein said contacts on said microelectronic element are disposed in a first region of said first surface, said compliant layer overlies a second region of said first surface, and one or more edge surfaces include one or more border edge surfaces extending along one or more borders between said first and second regions.

23. The method as claimed in claim 21, wherein said selectively forming bond ribbons step includes selectively electroplating said bond ribbons.

24. The method as claimed in claim 21, wherein said selectively forming bond ribbons step includes electrolessly plating a conductive material over the top of said assembly and selectively etching away said conductive material.

25. The method as claimed in claim 21, further comprising the step of:

before the providing a compliant layer step, providing a first dielectric protective layer on the first surface of the microelectronic element, the first dielectric layer having a plurality of apertures therein so that said contacts are accessible therethrough, the providing the compliant layer step including the step of providing the compliant layer over said first dielectric protective layer.

26. The method as claimed in claim 25, the selectively forming flexible bond ribbons step including selectively electroplating said bond ribbons atop said first dielectric protective layer and said compliant layer.

27. The method as claimed in claim 21, further including the step of providing a dielectric cover layer over said compliant layer and said bond ribbons after the step of selectively forming the bond ribbons, wherein the cover layer has a plurality of apertures so that said terminals are accessible therethrough.

28. The method as claimed in claim 21, further including the step of providing an encapsulant layer over ~~the~~ an exposed surface of the bond ribbons.

29. The method as claimed in claim 28, further including the step of providing a second dielectric protective layer atop the encapsulant layer wherein the second dielectric protective layer has a plurality of apertures so that said terminals are accessible therethrough.

30. The method as ~~claimed~~ in claim 21, further including the step of depositing a barrier metal atop said contacts, prior to the step of forming the bond ribbons, whereby the barrier metal helps to prevent voiding between the contacts and the bond ribbons.

31. The method as claimed in claim 21, the method being applied to a plurality of undiced semiconductor chips on a wafer to form a corresponding plurality of compliant semiconductor chip packages, the method further including the step of separating the packages following the step of depositing the bond ribbons.

32. The method as claimed in claim 21, the method being applied to a plurality of adjacent semiconductor chips arranged in an array to form a corresponding multiplicity of compliant semiconductor chip packages, the method